## REMARKS

Upon entry of this amendment, claims 1-3 and 5-7 are all the claims pending in the application. Claim 4 has been canceled by this amendment.

### I. Claim Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected claims 1-7 under 35 U.S.C. §103(a) as being unpatentable over Hansen (U.S. 5,832,263) in view of Hiromichi (JP 8-305634).

Claim 1, as amended, recites the feature of a cache controller for setting, if the data is stored, without being copied to the RAM, in the cache as cache data from the non-volatile memory, all dirty bits of cache tags associated with the cache data to "dirty". Applicants respectfully submit that the combination of Hansen and Hiromichi does not teach or suggest at least this feature of claim 1.

Regarding Hansen, Applicants note that this reference discloses a method for allowing modification of data that is stored in a non-modifiable storage unit (see col. 2, lines 14-16). For example, as explained in Hansen, the method involves intercepting a file access of a non-modifiable storage unit (or read-only storage unit) and using an associated modifiable storage unit to track and record all modifications made to the information stored in the non-modifiable storage unit (see col. 3, lines 57-61).

In particular, as shown in Fig. 1 of Hansen, when a user attempts to read information from the non-modifiable storage unit, the request is intercepted, and the modifiable storage unit is searched for entries which would affect the information corresponding to the read request (see Fig. 1, item 12; and col. 3, line 65 through col. 4, line 2). If no entries are found, the read request

is passed unchanged to the non-modifiable storage unit, but if any entry encompasses the requested information, the read request is diverted to the modifiable storage unit and modifying information is retrieved from the modifiable storage unit (see Fig. 1 and col. 4, lines 2-9).

Thus, in Hansen, by providing the ability to add modifying information (which may supplement, alter or delete information from the non-modifiable storage unit), the information that will be provided to the user, in response to a read request, will be different from the data stored in the non-modifiable storage unit (e.g., certain words, phrases or graphics may be suppressed) (see col. 4, lines 17-23).

Regarding Hiromichi, Applicants note that this reference discloses an information processing system having a cache memory 17, a main memory, and a ROM which stores at least a basic input/output program (see Abstract). In Hiromichi, a copy of the information in the ROM is stored in the cache memory 17 such that quick access to the information stored in the ROM is made possible (see Abstract).

In the Office Action, Applicants note that the Examiner has taken the position that all data in the cache is victimized to the main memory of the system once the cache runs out of space and that it is normal for a cache controller to set all dirty bits of cache tags to "dirty" (see Office Action at pages 3 and 4). Applicants respectfully disagree.

In particular, Applicants note that not all pieces of data in a cache are written to the main memory when the cache runs out of space. Instead, Applicants note that only pieces of data in the cache whose dirty bits are set to "dirty" would be written in the main memory. Further,

contrary to the assertion of the Examiner, Applicants note that it is not the normal duty of a cache controller to set all dirty bits of cache tags to "dirty".

In view of the foregoing, Applicants respectfully submit that while Hansen discloses the ability to modify data that is stored in a non-modifiable storage unit, and Hiromichi discloses the ability to copy information stored in a ROM to a cache memory, that neither Hansen nor Hiromichi discloses or suggests that a cache controller is provided for setting, if data is stored, without being copied to the RAM, in the cache as cache data from the non-volatile memory, all dirty bits of cache tags associated with the cache data to "dirty", as recited in amended claim 1.

Therefore, Applicants respectfully submit that the combination of Hansen and Hiromichi does not teach, suggest or otherwise render obvious all of the features recited in amended claim 1. Accordingly, Applicants submit that claim 1 is patentable over the cited prior art, an indication of which is kindly requested. Claims 2, 3, 5 and 6 depend from claim 1 and are therefore considered patentable at least by virtue of their dependency.

Regarding claim 7, Applicants note that this claim has been amended to recite the feature of setting, if data is, without being copied to the RAM, stored in the cache as cache data from the non-volatile memory, all dirty bits of cache tags associated with the cache data to "dirty".

For at least similar reasons as discussed above with respect to claim 1, Applicants respectfully submit that the combination of Hansen and Hiromichi does not teach, suggest or otherwise render obvious such a feature. Accordingly, Applicants submit that claim 7 is patentable over the cited prior art, an indication of which is kindly requested.

## II. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may best be resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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